

REMARKS

At the outset, Applicants thank the Examiner for the thorough review and consideration of the pending application. The Office Action dated July 12, 2004 has been received and its contents carefully reviewed.

Claims 1, 27, and 32 are hereby amended; and claims 24-26 and 28-31 are hereby canceled. Accordingly, claims 1-13, 15-23, 27, and 32-60 are currently pending. Reexamination and reconsideration of the pending claims is respectfully requested.

In the Office Action, the Examiner objected to claim 1 due to an informality; rejected claim 1 under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention; rejected claims 1-12 and 25-31 under 35 U.S.C. § 103(a) as being unpatentable over Gu et al. (U.S. Pat. No. 6,359,672) in view of Shimada et al. (U.S. Patent No. 6,147,722); objected to claims 24, 32, and 43 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the elements of the base claim and any intervening claims; and allowed claims 13, 15-23, 33-42, and 44-60.

Applicants appreciate the allowance of claims 13, 15-23, 33-42, and 44-60 and the indication of allowable subject matter in claims 24, 32, and 43.

The objection to claim 1 due to an informality is traversed and reconsideration is respectfully requested in view of the amendment made to claim 1 above.

The rejection of claim 1 under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention, is traversed and reconsideration is respectfully requested.

Rejecting claim 1, the Examiner asserts the terms “optimal and minimal” are relative terms which render the claim indefinite. Without reaching the merits of this assertion, Applicants hereby amend claim 1 to remove the aforementioned terms and submit the present rejection under 35 U.S.C. § 112, second paragraph, is moot. Consequently, Applicants

respectfully request withdrawal of the present rejection under 35 U.S.C. § 112, second paragraph.

The rejection of claims 1-12 and 25-31 under 35 U.S.C. § 103(a) as being unpatentable over Gu et al. in view of Shimada et al. is traversed and reconsideration is respectfully requested.

Claim 1 is patentable over Gu et al. in view of Shimada et al. in that claim 1 recites a combination of elements including, for example, “forming the pixel electrode on the organic insulating film so as to be overlapped, by a predetermined area, with the gate line and the data line, wherein a parasitic capacitance in an overlapping area between the pixel electrode and the data line is different from a parasitic capacitance in an overlapping area between the pixel electrode and the gate line.” Neither Gu et al. nor Shimada et al., singly or in combination, teach or suggest at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that claims 2-6 and 27, which depend from claim 1, are also patentable over Gu et al. in view of Shimada et al.

Claim 7 is patentable over Gu et al. in view of Shimada et al. in that claim 7 recites a combination of elements including, for example, “a pixel electrode formed on the organic insulating film and connected to a source electrode of the thin film transistor, said pixel electrode overlapping the gate line and the data line, wherein a parasitic capacitance in an overlapping area between the pixel electrode and the data line is different from a parasitic capacitance in an overlapping area between the pixel electrode and the gate line.” Neither Gu et al. nor Shimada et al., singly or in combination, teach or suggest at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claims 8-12, which depend from claim 7, are also patentable over Gu et al. in view of Shimada et al.

In rejecting claim 7, the Examiner states Gu et al. teaches that “parasitic capacitance is created at overlapped areas (col. 2, lines 7-21)” and that there is a “relationship between the parasitic capacitance and the thickness of the layer, dielectric constant and the area of the overlap (col. 5, lines 45-61).” The Examiner then acknowledges that Gu et al. “does not teach that the parasitic capacitance in an overlapping area between the pixel electrode and the data line is different from a parasitic capacitance in an overlapping area between the pixel electrode and the

gate line” apparently because “[t]he overlapped areas... [of Gu et al.] are similar and hence the parasitic capacitance is the same between the areas of overlap of the pixel electrode with either the data line or the gate line.” Attempting to cure the deficiency of Gu et al., the Examiner cites Shimada et al. as disclosing “different overlapped widths of the pixel electrodes with the gate and data lines (Fig. 3A) and (col. 12, lines 1-52)” and surmises “if one takes into consideration the different widths for the overlapped areas as taught by Shimada and calculates the parasitic capacitance... [from] the equation of Gu (col. 5, line 55), one can easily get that the parasitic capacitance in an overlapping area between the pixel electrode and the data line is different from a parasitic capacitance in an overlapping area between the pixel electrode and the gate line.” Applicants, however, respectfully disagree.

Specifically, the equation presented at column 5, line 55 of Gu et al. describes the relationship of parasitic capacitance with the dielectric constant of an insulation layer, the thickness of the insulation layer, and the area of overlap between two conductors. The equation used in Gu et al., however, is silent as to any relationship between widths of overlapping areas. Thus, without more information (i.e., the length of overlapping areas), Applicants respectfully submit one cannot “easily get that the parasitic capacitance in an overlapping area between the pixel electrode and the data line is different from a parasitic capacitance in an overlapping area between the pixel electrode and the gate line,” as asserted by the Examiner.

Concluding the rejection of claim 7, the Examiner states it would have been obvious to “have different parasitic capacitances at the overlapped areas as taught by Shimada to achieve excellent display characteristics and high aperture ratio devices (col. 1, lines 10-12 and col. 2, lines 46-50).” Again, Applicants respectfully disagree.

Obviousness can only be established by combining or modifying reference teachings to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the references also suggest the desirability of the combination. Thus, a *prima facie* case of obviousness can only be

established via some objective reason to combine the reference teachings. See M.P.E.P. 2143.01.

Assuming *arguendo* that Shimada et al. teaches different parasitic capacitances at overlapping areas of the pixel electrode and the gate and data lines, and even if the device of the device of Shimada et al. achieves excellent display characteristics and a high aperture ratio, as asserted by the Examiner, Applicants respectfully submit such advantages are not attributable to the mere fact that the parasitic capacitance between the pixel electrode and the gate line is allegedly different from the parasitic capacitance between the pixel electrode and the data line. For example, Shimada et al. teaches that the device achieves a high aperture ratio simply because the amount by which the pixel electrode overlaps underlying conductive lines is minimized (i.e., by minimizing the enlargement of light-shading regions) (see, for example, Shimada et al. at column 13, lines 44-48; column 15, lines 25-28; column 16, lines 54-58; column 18, lines 18-21, 46-67; and column 20, lines 23-26, 63-67). Further, Shimada et al. apparently obtains “excellent display characteristics” as a result of preventing light leakage within reverse tilt domains (see, for example, Shimada et al. at column 13, lines 41-44; column 15, lines 22-25; and column 16, lines 51-54). In view of the actual teachings of Shimada et al., Applicants respectfully submit one of ordinary skill in the art would not attribute the asserted advantages of Shimada et al. not to an alleged existence of different parasitic capacitances between different overlapping conductors, but to preventing light leakage within reverse tilt domains and minimizing the enlargement of light-shading regions. Therefore, it is submitted that proffered motivation is insufficient to establish a *prima facie* case of obviousness as the advantages of Shimada et al. would not be transferred to Gu et al. merely by ensuring that the parasitic capacitance in an overlapping area between the pixel electrode and the data line is different from a parasitic capacitance in an overlapping area between the pixel electrode and the gate line, as allegedly shown in Shimada et al.

In view of the above, Applicants respectfully submit there is no objective reason, absent impermissible hindsight reasoning, to modify Gu et al. with Shimada et al. as suggested by the Examiner and request withdrawal of the present rejection of claims 7-12 under 35 U.S.C. § 103(a).

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: October 12, 2004

Respectfully submitted,

By Valerie P. Hayes ^{Reg. No} 53,005
for Kurt M. Eaton
Registration No.: 51,640
MCKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006